UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
08/699,844	08/20/1996	DAVID R. DETTMER	18799.79(TT1	3703

7590 07/07/2004

CRAWFORD PLLC
1270 NORTHLAND DRIVE
SUITE 390
MENDOTA HEIGHTS, MN 55120

EXAMINER	
SWERDLOW, DANIEL	
ART UNIT	PAPER NUMBER
2644	35

DATE MAILED: 07/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	08/699,844	DETTMER, DAVID R.	
	Examiner	Art Unit	
	Daniel Swerdlow	2644	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 April 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4,7-9 and 24-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,7-9,24-28 and 32* is/are rejected.

7)☒ Claim(s) *29-31,33 and 34* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over McCaslin (US Patent 5,668,794) in view of Barron (US Patent 5,357,567).

3. Claim 1 claims a duplex portable handset speakerphone comprising a microprocessor. McCaslin discloses a speakerphone system (Fig. 1; Fig. 19) that allows full-duplex operation (column 21, lines 63-67). Claim 1 further claims the speakerphone comprises a hands-free receive register coupled to the microprocessor. McCaslin discloses an IIR peak detector (Fig. 20, reference 420; column 22, lines 6-7) that corresponds to the hands-free receive register claimed and receives a far-end signal (Fig. 19, reference $R_{in[k]}$ column 21, lines 53-54). Claim 1 further claims the speakerphone comprises a hands-free transmit register coupled to the microprocessor. McCaslin discloses an IIR peak detector (Fig. 20, reference 428; column 22, lines 35-38) that corresponds to the hands-free transmit register claimed and receives a near-end signal (Fig. 19, reference $S_{in[k]}$ column 22, lines 35-38). Claim 1 further claims the speakerphone comprises a first analog-to-digital converter coupled to the hands-free receive register. McCaslin discloses an analog-to-digital converter (Fig. 1, reference 12; column 5, lines 36-39) that corresponds to the first analog-to-digital converter claimed and is coupled to the IIR peak detector (Fig. 20, reference 420) via the Rin(k) signal. Claim 1 further claims the

speakerphone comprises a second analog-to-digital converter coupled to the hands-free transmit register. McCaslin discloses an analog-to-digital converter (Fig. 19, reference 34; column 5, lines 47-49) that corresponds to the second analog-to-digital converter claimed and is coupled to the IIR peak detector (Fig. 20, reference 428) via the Sin(k) signal. Claim 1 further claims the speakerphone comprises a first programmable digital attenuator in a speech path and coupled to the microprocessor and to a speaker. McCaslin discloses a variable attenuator (Fig. 19, reference 410; column 21, lines 41-42) that corresponds to the first programmable digital attenuator claimed and is in the speech path to the speaker (Fig. 19, reference 24). Claim 1 further claims the speakerphone comprises a second programmable digital attenuator in a speech path and coupled to the microprocessor and to a microphone. McCaslin discloses a variable attenuator (Fig. 19, reference 412; column 21, lines 43-45) that corresponds to the second programmable digital attenuator claimed and is in the speech path to a microphone (Fig. 19, reference 26). Claim 1 further claims the microprocessor alternately receives speech signals in the respective speech paths and determines peak volume levels on both speech paths. McCaslin discloses receiving a speech signal on each speech path during each sample period (i.e., alternately) and determining far end (column 22, lines 9-10) and near end (column 22, lines 36-38) signal power using peak signal. Claim 1 further claims the microprocessor adjusts gain levels in the speech paths in response to the peak volume levels. McCaslin discloses setting the attenuators in response to a power ratio derived from peak signal levels (column 22, line 66 through column 23, line 20). Claim 1 further claims the speakerphone comprises a memory circuit having an algorithm executable by the microprocessor for operating the speakerphone. While McCaslin discloses an echo suppressor and echo canceller configuration (Fig. 19, reference 414, 408) that

performs the functions of the microprocessor claimed and a method of setting attenuation that corresponds to the algorithm claimed, McCaslin fails to explicitly disclose the microprocessor, memory circuit and algorithm storage. One skilled in the art wishing to practice the echo suppressor taught by McCaslin would need to utilize appropriate hardware to implement the functions of the echo suppressor, an algorithm to operate the hardware and a memory in which to store the algorithm. Barron discloses use of the microprocessor and storage of an algorithm in a memory to implement echo suppression (Fig. 1, reference 115, 160, 135, 130; column 3, lines 13-29). It would have been obvious to one skilled in the art at the time of the invention to apply the microprocessor, memories and algorithm storage as taught by Barron to the echo suppressor taught by McCaslin for the purpose of implementing the echo suppressor in a physical platform.

4. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over McCaslin in view of Barron and further in view of Chen et al. (US Patent 5,075,687).

5. Claim 2 is essentially similar to Claim 1 with the exception that Claim 2 additionally claims a pre-amplifier coupled to the microprocessor, a codec instead of analog-to-digital converters and consolidation of the microprocessor, hands-free registers, pre-amplifier, codec and attenuators on an integrated circuit controller chip. As stated above apropos of Claim 1, the combination of McCaslin and Barron makes obvious all elements of that claim. In addition, the analog-to-digital and digital-to-analog converter combination disclosed by McCaslin (Fig. 19, references 16, 34) constitutes a codec. Therefore, the combination makes obvious all elements of Claim 2 with the exception of a pre-amplifier coupled to the microprocessor and consolidation of the microprocessor, hands-free registers, pre-amplifier, codec and attenuators on an integrated

circuit controller chip. Chen discloses integration of the speakerphone hardware on a single integrated circuit (column 2, lines 20-22; column 1, lines 25-44) that corresponds to the integrated circuit controller chip claimed. It would have been obvious to one skilled in the art at the time of the invention to apply integration as taught by Chen to the circuit disclosed by Barron for the purpose of reducing cost and improving stability, sensitivity and consistency. Therefore the combination of McCaslin, Barron and Chen is shown to make obvious all elements of Claim 2 with the exception of a pre-amplifier coupled to the microprocessor. Chen discloses a booster amplifier (Fig. 1, reference 28; column 3, lines 3-7) that corresponds to the pre-amplifier claimed and is coupled to a control circuit that corresponds to the microprocessor claimed. It would have been obvious to one skilled in the art at the time of the invention to apply the booster amplifier taught by Chen to the combination made obvious by McCaslin, Barron and Chen for the purpose of creating a better quality transmitted signal by increasing the signal-to-noise ratio at the input to the analog-to-digital converter.

6. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over McCaslin in view of Barron and further in view of Chen as applied to Claim 2 above, and further in view of Teitler et al. (US Patent 5,722,086). Claim 4 claims the system of Claim 2, further including a base station comprising an integrated circuit controller chip comprising a codec, a telephone line interface and a radio frequency interface. As stated above apropos of Claim 2, the combination of McCaslin, Barron and Chen makes obvious all elements of that claim. Therefore, the combination makes obvious all elements of Claim 4 with the exception of a base station comprising an integrated circuit controller chip comprising a codec, a telephone line interface and a radio frequency interface. Teitler discloses a system including a base station (Fig. 1,

reference 14; column 2, lines 9-12) comprising a microcontroller unit (Fig. 1, reference 28; column 2, lines 39-46) that corresponds to the controller claimed, an ADPCM decoder and ADPCM decoder D/A combination (Fig. 1, reference 26, 34; column 2, lines 31 through 39) that corresponds to the codec claimed, an output signal to a telephone system (column 2, lines 54-57) that corresponds to the telephone line interface claimed, and an RF interface (Fig. 1, reference 24; column 2, lines 34-39) that corresponds to the radio frequency interface claimed. It would have been obvious to one skilled in the art at the time of the invention to apply the RF and telephone interface functions and the codec and controller functions as taught by Teitler to the combination of McCaslin, Barron and Chen for the purpose of increasing convenience and allowing the speakerphone to be used at a location a distance from a hard wired telephone connection without hazardous and unsightly cords by making the full duplex speakerphone cordless. Therefore, the combination of Barron, Chen and Teitler is shown to meet all elements of Claim 4 with the exception of the codec function being included in a controller chip. Teitler discloses the combination of codec and control functions on an ADPCM CODEC chip (column 3, lines 41-44). It would have been obvious to one skilled in the art at the time of the invention to apply the ADPCM CODEC chip as taught by Teitler to the combination taught by Barron, Chen and Teitler for the purpose of making shipping and assembly cheaper by reducing the size and component count of the base unit.

7. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over McCaslin in view of Barron and further in view of Teitler.

8. All elements of Claim 7 are comprehended by Claim 1 with the exception that Claim 7 claims a ROM containing a stored operation algorithm for directing the microprocessor and a

radio frequency interface at one end of each speech path. As stated above apropos of Claim 1, the combination of McCaslin and Barron makes obvious all elements of that claim. In addition, Barron discloses a ROM (Fig. 1, reference 130) for storing software to implement the speakerphone functions (column 10, lines 48-52). It would have been obvious to one skilled in the art at the time of the invention to apply algorithm storage in ROM as taught by Barron to the combination made obvious by McCaslin and Barron for the purpose of improving reliability by maintaining the algorithm in memory through a power interruption. Therefore the combination of McCaslin and Barron makes obvious all elements of Claim 7 with the exception of a radio frequency interface at one end of each speech path. Teitler discloses an RF interface (Fig. 1, reference 22; column 2, lines 12-16) that corresponds to the radio frequency interface claimed. It would have been obvious to one skilled in the art at the time of the invention to apply an RF interface as taught by Teitler to the combination of McCaslin and Barron for the purpose of increasing convenience and allowing the speakerphone to be used at a location a distance from a hard wired telephone connection without hazardous and unsightly cords by making the speakerphone cordless.

9. Claim 8 claims the method of Claim 7 wherein the stored operation algorithm uses software timers and peak detection. As stated above apropos of Claim 7, the combination of McCaslin, Barron and Teitler meets all elements of that claim. In addition, McCaslin discloses peak detection (column 22, lines 9-10 and 36-38) and determination of peak speech amplitude over predetermined sample times (column 3, lines 59-64). Further, McCaslin discloses the use of software timers (column 14, lines 40-42).

10. Claims 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over McCaslin in view of Barron and further in view of Teitler as applied to Claim 8 above and further in view of Intel (80C186EA/80C188EA Microprocessor User's Manual).

11. Claim 9 claims the method of Claim 8 wherein a software timer generates a hardware interrupt to the microprocessor every speech frame so that one of the hands-free registers can be read by a software peak detector. As shown above apropos of Claim 1, McCaslin discloses repeated recalculation of attenuation based on peak detection (Fig. 20, reference 420, 428) performed by an IIR filter algorithm. However, McCaslin is silent on the details of the peak detection algorithm. As such, one skilled in the art seeking to practice the echo suppressor of McCaslin would be motivated to seek a peak detection algorithm. Barron discloses a peak detection algorithm (Fig. 5; column 5, lines 32-35) that operates on consecutive speech samples (i.e., frames). That is, the software peak detection of Barron reads the respective values on the transmit and receive lines once every sample period. It would have been obvious to one skilled in the art at the time of the invention to apply the peak detection algorithm taught by Barron to the combination of McCaslin, Barron and Teitler for the purpose of performing the peak detection function. Therefore, the combination is shown to make obvious all elements of Claim 9 except the use of a software timer to generate a hardware interrupt to the microprocessor every speech frame to trigger the reading of the line values. In disclosing the peak detection algorithm, Barron is silent as to the way the algorithm is activated to take in each speech sample. Since it was well known that speech samples occur periodically, one skilled in the art would have been motivated to seek a way of generating a periodic signal to trigger the sample reading in the algorithm disclosed by Barron. Intel discloses the use of software timers to generate periodic

hardware interrupts (pp. 9-16 through 9-20). It would have been obvious to one skilled in the art at the time of the invention to apply the use of software timers to generate periodic hardware interrupts as taught by Intel to the combination of McCaslin, Barron and Teitler for the purpose of triggering the sample reading in the algorithm disclosed by Barron.

12. Claims 24, 26 through 28 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over McCaslin in view of Teitler.

13. Claim 24 claims a speakerphone arrangement comprising a base unit and a portable handset communicatively coupled to the base unit via a wireless channel, including a microphone and a speaker. McCaslin discloses a speakerphone system (Fig. 1; Fig. 19) comprising a microphone (Fig. 19, reference 26) and a speaker (Fig. 19, reference 24). Claim 24 further claims the arrangement comprises a first speech path to the speaker. McCaslin discloses a speech path (Fig. 1, reference 10, 12; Fig. 19, reference 400, 410, 16, 22) to the speaker (Fig. 19, reference 24). Claim 24 further claims the arrangement comprises a second speech path to the microphone. McCaslin discloses a speech path (Fig. 1, reference 15, 48; Fig. 19, reference 402, 412, 44, 38, 36, 34, 30, 28) to the microphone (Fig. 19, reference 26). Claim 24 further claims the arrangement comprises a first programmable digital level-adjuster adapted to be controlled to provide a gain adjustment along the first speech path. McCaslin discloses a variable attenuator (Fig. 19, reference 410; column 21, lines 41-42) that corresponds to the first programmable digital level adjustor claimed and is in the speech path to the speaker (Fig. 19, reference 24) and is controlled to insert attenuation (i.e., provide gain adjustment) in that path (column 21, lines 41-52). Claim 24 further claims the arrangement comprises a second digital

level-adjuster adapted to be controlled to provide a gain adjustment along the second speech path. McCaslin discloses a variable attenuator (Fig. 19, reference 412; column 21, lines 43-45) that corresponds to the second programmable digital level adjustor claimed and is in the speech path to the microphone (Fig. 19, reference 26) and is controlled to insert attenuation (i.e., provide gain adjustment) in that path (column 21, lines 41-52). Claim 24 further claims the arrangement comprises a logic decision circuit coupled to the programmable digital level adjusters and adapted to alternately receive speech signals in the respective speech paths. McCaslin discloses an echo suppressor (Fig. 19, reference 414) that corresponds to the logic decision circuit claimed, is coupled to the variable attenuators (Fig. 19, reference 410, 412) that correspond to the programmable digital level adjusters claimed and receives a speech signal on each speech path during each sample period (i.e., alternately) (column 22, lines 9-10, 36-38). Claim 24 further claims the logic decision circuit being adapted to regularly determine the respective peak amplitudes of signals in the first and second speech paths and control the gains in the paths by controlling the programmable digital level adjusters during full duplex operation. McCaslin discloses setting the attenuators in response to a power ratio derived from peak signal levels (column 22, line 66 through column 23, line 20) during full duplex operation (column 21, lines 62-67). Therefore, McCaslin anticipates all elements of Claim 24 with the exception of the arrangement comprising a base unit and a portable handset communicatively coupled to the base unit via a wireless channel. Teitler discloses a telephone arrangement comprising a base station and a handset (Fig. 1, reference 14, 12; column 1, lines 53-54) connected by a wireless link. It would have been obvious to one skilled in the art at the time of the invention to apply wireless interconnection as taught by Teitler to the system taught by McCaslin for the purpose of

increasing convenience and allowing the speakerphone to be used at a location a distance from a hard wired telephone connection without hazardous and unsightly cords by making the speakerphone cordless.

14. Claim 26 claims the arrangement of Claim 24 wherein the logic decision circuit is configured and arranged to dynamically regulate the balance of the speech paths during full duplex operation. As stated above apropos of Claim 24, the combination of McCaslin and Teitler makes obvious all elements of that claim. In addition, McCaslin discloses controlling the attenuation in both speech paths based on the signals on both paths (column 21, lines 58-62). Therefore, the combination of McCaslin and Teitler makes obvious all elements of Claim 26.

15. Regarding Claims 27 and 28, Claim 27 claims the arrangement of Claim 24 wherein the logic decision circuit is further adapted to implement automatic gain control and thereby regulate gain proportions on at least one of the two speech paths in a full duplex state. While Claim 28 claims regulation of gain proportions along both speech paths. As stated above apropos of Claim 24, the combination of McCaslin and Teitler makes obvious all elements of that claim. In addition, McCaslin discloses controlling the attenuation in both speech paths based on the signals on both paths (column 21, lines 58-62). Since the resulting gain control is implemented automatically, the combination of McCaslin and Teitler makes obvious all elements of Claims 27 and 28.

16. Claim 35 is essentially similar to Claim 24 and is rejected for the reasons stated above apropos of Claim 24.

17. Claims 25 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over McCaslin in view of Teitler as applied to Claim 24 above, and further in view of Barron.

18. Claim 25 claims the arrangement of Claim 24 wherein the logic decision circuit is a microprocessor circuit. As stated above apropos of Claim 24, the combination of McCaslin and Teitler makes obvious all elements of that claim. While McCaslin discloses an echo suppressor and echo canceller that correspond to the logic decision circuit, McCaslin fails to explicitly disclose specific physical details of these elements. One skilled in the art wishing to practice the echo suppressor taught by McCaslin would need to utilize appropriate hardware to implement the functions of the echo suppressor. As stated above apropos of Claim 1, Barron discloses use of the microprocessor to implement echo suppression. It would have been obvious to one skilled in the art at the time of the invention to apply the microprocessor taught by Barron to the combination made obvious by McCaslin and Teitler for the purpose of implementing the echo suppressor in a physical platform.

19. Claim 32 claims the arrangement of Claim 24 wherein the logic decision circuit is further adapted to implement automatic gain control using hysteresis and thereby regulate gain proportions along both speech paths in a full duplex state. As stated above apropos of Claim 24, the combination of McCaslin and Teitler makes obvious all elements of that claim. In addition, as stated above apropos of Claim 28, McCaslin discloses implementation of automatic gain control on both speech paths. Therefore, the combination of McCaslin and Teitler makes obvious all elements of Claim 32 with the exception of hysteresis. Barron discloses the use of hysteresis (column 6, lines 1-10) in implementing gain control. It would have been obvious to

one skilled in the art at the time of the invention to apply hysteresis as taught by Barron to the combination made obvious by McCaslin and Teitler for the purpose of reducing choppiness.

Allowable Subject Matter

20. Claims 29 through 31, 33 and 34 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

21. The following is a statement of reasons for the indication of allowable subject matter: Claim 29 claims operation in a plurality of full duplex substates, each substate defining a different relationship between the respective speech path gains. While McCaslin discloses a coordinated variation of the gains in each speech path and transitions between operating modes based on signal levels in the speech paths (column 24, lines 6-22), the variation disclosed by McCaslin is continuous over a range of gains for each path. McCaslin does not disclose substates, each with a particular gain combination. Since the prior art neither anticipates nor makes obvious this element, claim 29 is allowable matter.

22. Claims 30 and 31 are allowable matter due to dependence from Claim 29.

23. Claim 33 is essentially similar to Claim 31 and is allowable matter for reasons stated above apropos of that claim.

24. Claim 34 claims operation in a plurality of full duplex substates, with transition between the substates based on volume levels in the speech paths and the current substate. While McCaslin discloses transitions between operating modes based on signal levels in the speech paths (column 24, lines 6-22), McCaslin does not disclose basing the transitions on a current

substate. Since the prior art neither anticipates nor makes obvious this element, claim 34 is allowable matter.

Response to Arguments

25. Applicant's arguments filed on 30 April November 2004 have been fully considered but they are not persuasive.

26. Spanning pages 8 and 9 of the response, applicant states:

> In direct contrast to the teachings of the claimed invention, the Examiner has made a hypothetical "prior art" combination of references that would replace the algorithm and approach of the [McCaslin] '794 reference with a microprocessor-implemented approach that directly undermines the purpose of the '794 reference. Specifically, the purpose of the '794 reference involves using a particular variable gain algorithm for implementing echo suppression. See, e.g., column 27, line 66 through column 28, line 12. The Examiner's suggestion that a skilled artisan would be motivated to replace the algorithm and corresponding circuit components of the '794 reference with the microprocessor-implemented approach of the [Barron] '567 reference is therefore untenable.

27. As stated in the claim rejections above, it is well established that the determination of obviousness includes evaluation of the prior art from the standpoint of a hypothetical person of ordinary skill in the art. As such, a determination of obviousness may involve "hypothetical prior art" since the actual existence of a combination that comprises all elements of a claim would be anticipation. Applicant's characterization of the combination of McCaslin and Barron as "hypothetical prior art" does not invalidate determination of the obviousness of the claimed invention in view of that combination.

28. Further, applicant mischaracterizes the combination in stating it "would replace the algorithm and approach of the '794 reference with a microprocessor-implemented approach that directly undermines the purpose of the '794 reference." A microprocessor implemented

approach does not replace an algorithm. Rather, a microprocessor implemented approach implements an algorithm. In order to practice the algorithm disclosed in McCaslin, one skilled in the art would have needed to create a physical apparatus. The motivation for the combination stems from this need. Barron demonstrates the suitability of the microprocessor for implementing a gain control algorithm. The application of the microprocessor does not "replace the ... corresponding circuit components of the '794 reference" because the reference does not teach circuit components. Rather, the reference teaches functional blocks that perform complicated mathematical operations such as peak detection, noise estimation, normalization, ratio calculation, encoding and table lookups. Applicant's allegation that applying microprocessor implementation as taught by Barron to this algorithm undermines the purpose of the McCaslin reference is, therefore, unfounded.

29. Applicant further states:

> Moreover, the proposed modification of the primary '794 reference does not address the shortcomings of the '794 reference because the asserted combination still fails to teach or suggest claimed limitations including alternately receiving speech signals in respective speech paths, as well as full duplex operation.

30. As stated in the Claim rejections above, McCaslin discloses receiving a speech signal on each speech path during each sample period and determining far end (column 22, lines 9-10) and near end (column 22, lines 36-38) signal power using peak signal. The speech signals are designated Rin(k) and Sin(k) where k is an index designating a particular sample. As such, every sample on each line is received. Because both signals are sampled at the same rate, there is one far end sample for every near end sample and one near end sample for every far end sample. Since a microprocessor performs operations serially, it will necessarily alternate receiving the two signals.

31. Further, McCaslin discloses full duplex operation in column 21, lines 62-67, stating: "The attenuation levels are such that full-duplex communication is allowed such that, if both ends are talking at the same time, the attenuation will be minimized to minimize the source of the signal, thereby making both parties easy to understand. This is also the case when both sides are idle."

32. In the middle of page 9 of the response, applicant alleges:

> In an apparent attempt to overcome the deficiencies of the '794 reference relative to the claimed limitations of the instant invention, the Examiner simply stated that the "microprocessor, memories and algorithm storage taught by Barron" could be applied to the echo suppressor taught by the '794 reference. In addition, the Examiner further asserted, on page 4 of the Office Action, that the receipt of a speech signal on each speech path during each sample period with the '794 reference implies alternately receiving speech signals as claimed. However, as previously discussed, the Examiner has not shown how the '794 reference would be modified to include these limitations and thus has not shown how all of the cited elements would work together as claimed. For example, adding the "microprocessor, memories and algorithm storage taught by Barron" to the '794 reference would maintain the same operation taught by the '794 reference and thus does not provide correspondence to the claim limitations (e.g., alternately receiving speech signals) of the present invention.

33. As stated above, McCaslin teaches an algorithm for a variable gain echo suppressor used in a full duplex speakerphone. McCaslin discloses functional blocks and flow charts. In describing the flow charts, McCaslin repeatedly refers to "the program". One skilled in the art wishing to practice the invention disclosed in McCaslin would therefore have motivation to utilize a physical device that could execute such a program. Barron teaches the suitability of a microprocessor for such a purpose. Again, it is not a question of "modifying" McCaslin, but rather a matter of implementing McCaslin since McCaslin is silent as to physical realization of the disclosed invention.

34. Examiner has detailed above how the combination of McCaslin and Barron teaches alternately receiving speech signals as claimed.

35. Spanning pages 9 and 10 of the response, applicant alleges:

> More particularly, the Examiner has cited no portion of the '794 reference that would indicate that the receipt of a speech signal on each speech path during a sample period implies, as the Examiner asserts, alternately receiving speech signals, or that a microprocessor-implemented approach is contemplated. Rather, the sampling of speech signals in the incoming and outgoing speech paths in the '794 reference is concurrent and implemented with discreet components. There is no discussion in the cited portions of the '794 reference that would indicate that speech signals in different speech paths are alternately received. In addition, the algorithm of the '794 reference is implemented with discreet components as described, for example, in connection with FIG. 19. For instance, the cited portions of the '794 reference discussing the embodiments shown in FIG. 19 rely upon the double-talk detector 54 and adaptive filter 40 of FIG. I for implementing the echo canceller 408 (see, e.g., column 21, lines 30-35). The double-talk detector 54 is further discussed in connection with FIG. 2, and the adaptive filter 40 with FIG. 6, with reference to various discreet component implementations. Furthermore, in absence of a microprocessor and in view of the purposeful discrete circuit implementations discussed above, clearly the discreet approach of the '794 reference would involve the simultaneous sampling of speech signals in alternate paths. For instance, referring to FIG. 20, discrete peak detect circuits 420 and 428 are separately implemented and simultaneously sample signals in different speech paths; there is no teaching or suggestion of coordination between these discrete components. In this regard, the Examiner has not shown how the cited references teach all of the claim limitations and thus has failed to meet the correspondence requirement for establishing a prima facie Section 103 rejection.

36. Examiner has detailed above how the combination of McCaslin and Barron teaches alternately receiving speech signals as claimed. In addition, applicant mischaracterizes McCaslin as teaching an implementation using discrete components. McCaslin discloses functional blocks in Figs. 19 and 20 such as echo suppressor (414) and IIR (infinite impulse response) peak detector (420). These are clearly not discrete components. McCaslin characterizes Fig. 6 as a "block diagram", that is a representation of functions, not discrete components. As discussed above, a microprocessor is appropriate for implementation of the

functions disclosed by McCaslin. As such, the combination of McCaslin and Barron teaches each and every limitation of the claim.

37. In the middle of page 10 of the response, applicant alleges:

> The Examiner further failed to cite any evidence in support of the assertion that the proposed modification of the '794 reference would be motivated. Specifically, the Examiner asserted that, because the purpose of the modification is to implement "the echo suppressor in a physical platform," one of skill in the art would be motivated to do so. These mere allegations of motivation made in hindsight and without any supporting evidence do not meet the evidence requirement for establishing a prima facie Section 103 rejection. See, e.g., In re Dembiczak, 175 F.3d 994, 50 USPQ2d 1614 (Fed. Cir. 1999). See also In re Fine, 837 F.2d 1071, 1075, 5 USPQ2d 1596, 1600 (Fed. Cir. 1988) (evidence of teaching or suggestion "essential" to avoid hindsight). In this instance, the Examiner's conclusion that one of skill in the art would look to modify the '794 reference in this manner lacks evidence that would show why one of skill in the art would be motivated to embody the echo suppressor in the manner suggested by the Examiner. Therefore the Section 103 rejection fails to meet the motivation requirement for establishing a prima facie Section 103 rejection.

38. To show obviousness, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. By itself, the McCaslin reference teaches functional blocks and algorithms. No physical embodiment is disclosed. As such, there is motivation to provide a physical platform on which to implement the functions and algorithm taught by McCaslin. As shown by Barron, at the time of the invention it was well known to use a microprocessor for such a purpose. As such, McCaslin is evidence of motivation since additional teaching is required to practice the invention of McCaslin.

39. Spanning pages 10 and 11 of the response, applicant alleges:

> Moreover, the proposed modification would undermine the purpose of the relied upon embodiment of the '794 reference of achieving full-duplex operation while maintaining low-cost. See, e.g., column 3, lines 30-37 and column 7, lines 10-23, Where a proposed modification of a primary reference would undermine its purpose, there is no motivation to make the modification (see, e.g., In re Gordon, 733 F.2d 900 (Fed. Cir. 1984)). The Applicant has previously pointed out that the '794 reference has a purpose of low-cost

> implementation, in referencing the drawbacks of previous implementations of echo cancellation with an adaptive filter, The Examiner has pointed out, in the Response to Arguments section, that the '794 reference indeed uses a filter in certain embodiments. However, the Applicant has not asserted that this purpose of the '794 reference requires that no adaptive filter be used. Rather, the above-referenced portions of the '794 reference emphasize the reference's purposes of achieving full-duplex operation at low cost. While the '794 reference does employ an adaptive filter as pointed out by the Examiner, the implementation of the filter is effected in connection with this purpose, which would be undermined, were the proposed combination made.

40. Applicant erroneously states the purpose of the embodiment relied upon in McCaslin as maintaining low cost. While McCaslin discloses expense associated with echo canceling, it is clear that the purpose of the embodiment relied upon is to provide a communication system using an echo suppressor. In addition, as examiner has pointed out above, the use of a microprocessor is not a modification of McCaslin since McCaslin is silent as to the physical implementation of the embodiment. As such, the application of the teaching of Barron provides missing detail rather than any change. Further, applicant has provided no evidence that the microprocessor implementation is less economical than some hypothetical other implementation of McCaslin.

41. In the middle of page 11 of the response, applicant alleges:

> Regardless of whether the '794 reference employs an adaptive filter, the addition of the expensive programmed '567 processor (DSP56001), as well as the '567 memory circuit and its algorithm storage to the '794 reference would be contrary to the purpose of the '794 reference. The '794 reference teaches the utilization of the algorithm described at column 12, line 64 through column 13, line 14, with discrete circuitry (without a processor) being used to address the high speed data processing required to suppress the echo. In this regard, the Examiner's comments on page 15 in the Response to Arguments section of the Office Action, indicating the Applicant has no support for utilizing the algorithm with discrete circuitry, are incorrect. The cited portion of the '794 reference discussed by the Examiner refers to another U.S. Patent Application that involves the use of such discrete circuits. Furthermore, as discussed above, various other cited portions of the '794 reference specifically call out the use of discrete circuitry.

42. Again applicant mistakenly alleges that McCaslin teaches a discrete circuit implementation. As shown above, no such teaching exists in McCaslin. The portion of McCaslin cited by applicant reads in full:

> In order to accommodate a "radical path change" situation, a Variable Step Size algorithm is utilized, which is disclosed in U.S. Pat. No. 4,894,820 issued Jan. 16, 1990, which is incorporated herein by reference. In U.S. Pat. No. 4,894,820, this algorithm is utilized to control step size, whereas the present apparatus utilizes the algorithm to detect path changes. In the use of the Variable Step size algorithm in the present apparatus, for any particular tap in the adaptive filter, the update term for that tap will tend to have the same sign for each sample time during convergence of the filter. Once the filter has completed convergence, the sign of the update term will likely vary. The average value of the sign of this term will be zero. If the absolute value of the average of the sign of the update term exceeds a particular threshold, convergence is in progress. If it is below the threshold, convergence is declared complete. This algorithm facilitates a reduction in update gain once the adaptive filter has achieved a particular level of convergence.

Nowhere in the cited passage is discrete circuitry mentioned, let alone required. Nor does McCaslin disclose the use of any physical structure from U.S. Pat. No. 4,894,820. Rather McCaslin specifically discloses use of "a Variable Step Size algorithm is utilized, which is disclosed in U.S. Pat. No. 4,894,820". The fact that McCaslin discloses this as an algorithm and not a circuit is indicative of the lack of disclosure of physical embodiment in McCaslin and therefore the motivation to combine with the teaching of Barron.

43. Spanning pages 11 and 12 of the response, applicant alleges:

> Inserting the programmed '567 processor (DSP56001) as well as the '567 memory circuit and its algorithm storage into the heart of the '794 system would result in a much more expensive '794 system as well as replace this '794 circuitry and algorithm. It is also unclear as to whether the '794 system would operate as intended, were its circuitry and algorithm replaced; the Examiner has not shown how this replacement would function. Furthermore, the new half-duplex-switching algorithm of the '567 reference would destroy the full-duplex purpose of the '794 reference. This proposed modification of the '794 reference would thus undermine its purpose and therefore is unmotivated.

44. First, as stated above, the combination of McCaslin and Barron is not an alteration of McCaslin, but an implementation. Second, as evidenced by Barron, at the time of the invention,

microprocessor implementation of echo cancellation algorithms was well known and applicant has shown no evidence that the hypothetical discrete circuit implementation was more economical than the microprocessor implementation. Third, examiner has not suggested replacing the algorithm in McCaslin with the algorithm in Barron. Rather the combination of McCaslin and Barron implements the algorithm of McCaslin in a microprocessor, as taught by Barron and as such does not undermine the purpose of McCaslin. Finally, it is not necessary that examiner show how the combination would function. At the time of the invention, as evidenced by Barron, it was within the ability of one skilled in the art to implement a speakerphone algorithm on a microprocessor.

45. For these reasons, examiner maintains the rejections based on the combination of McCaslin and Barron.

46. In the third complete paragraph on page 12 of the response, applicant alleges:

> Regarding the Section 103 rejection of claim 2, Applicant submits that the Examiner failed to show correspondence between the cited references and every limitation in claim 2. For example, the Examiner asserts on page 5 of the Office Action that the "analog-to-digital and digital-to-analog converter combination" in FIG. 19 of the '794 reference constitutes a codec. However, the Examiner failed to show how this combination corresponds to the claimed limitations directed to a codec "having first and second programmable digital attenuators" in claim 2. Therefore, the Examiner failed to meet the requirement that all limitations be taught in order to establish a prima facie Section 103 rejection, and Applicant requests that the rejection be removed.

47. As shown above in the rejections of Claims 1 and 2, in the embodiment relied upon (Fig. 19) McCaslin discloses a codec in the form of the analog-to-digital and digital-to-analog converter combination (34, 16) and variable attenuators (i.e., programmable digital attenuators) (410, 412) associated with the codec signal paths. As such, McCaslin discloses "a codec having first and second programmable digital attenuators".

48. Spanning pages 12 and 13 of the response, applicant alleges:

> Further regarding the Section 103 rejection of claim 2, Applicant submits that the Examiner failed to cite evidence of motivation for making the asserted modifications of the primary '794 reference. Instead of citing evidence, the Examiner has made allegations of motivation in hindsight and without any support for the allegations. For example, on page 5 of the Office Action, the Examiner discusses that it "would have been obvious" to apply integration for "reducing cost and improving stability, sensitivity and consistency," On page 6 of the Office Action, the Examiner further discusses that adding a booster amplifier would have been obvious for "creating a better quality transmitted signal ...." As discussed above, without evidence in support of such allegations, there is no prima facie case for maintaining a Section 103 rejection and Applicant therefore requests that the rejection be removed.

49. To show obviousness there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. In this case, the motivation for integration comes from Chen (Column 1, lines 25-44):

> A significant portion of telephone equipment manufacturing costs may be attributable to parts and equipment assembly. One approach to reducing costs is to provide a low-cost part which requires no external components. Incorporation of external components into an integrated circuit generally yields a device which is more stable in its operation, has good sensitivity, and is consistent in its performance. Additional advantages are realized when the integrated circuit is a digital circuit. Principal among such additional advantages are even further improved stability and programmability of various operational parameters associated with the apparatus. Digital programmability provides a versatile apparatus which may be easily tailored to be applicable to a wide variety of operational environments using a single integrated design. As a result, the development costs and manufacturing costs associated with the apparatus are much reduced since they are able to be spread across a wider variety of products.

The motivation for use of the booster amplifier that corresponds to the preamplifier claimed is also found in Chen (column 3, lines 3-7):

> A booster amplifier 28 is included before analog attenuator 30 to increase the signal-to-noise ratio of the outgoing signal before it is treated by analog attenuator 30 or analog-to-digital conversion circuit 20.

And (column 3, lines 36-39):

> Booster amplifier 28 boosts the outgoing analog signal level before analog-to-digital conversion circuit 20 performs its analog-to-digital conversion in order to improve conversion performance.

As such, one skilled in the art would have motivation to use the booster amplifier to realize these benefits.

50. In the middle of page 13 of the response, applicant alleges:

> Regarding the Section 103 rejection of claims 8 and 9, the Examiner has also failed to show correspondence between the cited references and all claimed limitations. For example, the Examiner has failed to show where any reference teaches or suggests limitations directed to a software timer that generates a hardware interrupt on every speech frame so that a hands-free register can be read by a software peak detector. While the Examiner has mentioned, on page 8 of the Office Action, that the '794 reference discloses the use of software timers, the cited portion of the '794 reference does not disclose software times. In addition, the Examiner has not shown how this cited portion would correspond to other cited portions of the '794 reference that allegedly teach other claimed limitations including peak detection and determination of peak speech amplitude over predetermined sample times. Furthermore, the Examiner has failed to provide evidence of motivation for combining the multitude of references strung together to arrive at the alleged teachings. In attempting to show evidence of such motivation, the Examiner simply stated asserted advantages for the various secondary references and failed to provide evidence showing specifically why the primary '794 reference should be modified or why it would benefit from such alleged advantages. Without showing correspondence to all claimed limitations or proper evidence for modifying the '794 reference, there is no prima facie Section 103 rejection for claims 8 and 9 and Applicant requests that the rejection be removed.

51. The cited portion of McCaslin reads:

> After the time out has occurred, the program will flow from the decision block 202 along a "Y" path to a function block 204 to read the value in the accumulator.

A decision in a program based on a time out shows the use of a software timer. Claim 8 reads in full: "The method of claim 7, wherein the stored operation algorithm uses software timers and peak detection." No relationship is claimed between the software timers and other elements except that the software timers are used by a stored algorithm that directs the microprocessor. As such, claim 8 does not limit the software timers to uses included in the claims.

52. Claim 9 claims "a software timer generates a hardware interrupt to the microprocessor on every speech frame so that one of the hands-free registers can be read by a software peak

detector." As shown above in the rejection of Claim 9, the combination of McCaslin, Barron, Teitler and Intel makes obvious all elements of this claim. The motivation for combination of McCaslin and Barron is discussed above. In addition, the disclosure of peak detection by McCaslin without details provides motivation for one skilled in the art to seek a peak detection algorithm which is found in Barron, but requires periodic triggering without disclosure of how this is accomplished. As such, motivation exists to apply Intel's teaching of software timers and hardware interrupt to produce the triggering signal. As such, motivation to combine references stems directly from an attempt to practice the invention of McCaslin by one skilled in the art. Incorporating the limitations of the claims from which it depends, Claim 9 combines elements ranging from well known high level systems (e.g., a radio frequency interface) to well known low level software programming techniques (e.g., software timers). Because references are normally limited in scope to particular inventions, the fact that four references are required to span the wide scope of this claim is not an indication of impermissible hindsight. In this case, as has been shown, the references are complementary, filling in one another's areas lacking in detail. As such, it is possible that applicant's characterization of four references as "a multitude" is an exaggeration.

53. Spanning pages 13 and 14 of the response, applicant alleges:

> With respect to the Section 103 rejection of claims 24 and 35 over the '794 McCaslin reference in view of Teitler, Applicant respectfully traverses because the asserted prior art does not correspond to the claimed invention. The '794 reference is deficient in alleged teachings as discussed above in connection with the Section 103 rejection of claim 1 (and others having similar limitations). For instance, the cited portion of the '794 reference allegedly teaching limitations directed to "determining regularly the respective peak amplitudes of signals" fails to mention peak amplitude determination, In addition, the '794 reference has been misinterpreted as having an echo suppressor 414 that must alternately receive speech signals, respectively, in transmit and receive paths. Rather, the echo suppressor 414 of figure 19 of the '794

reference is shown and described in enlarged form via figure 20. In connection with figure 20, the '794 reference describes and illustrates the far end and near end portions of the echo suppressor 414 as being implemented in discrete paths and without any alternate signal receiving or other alternate processing.

54. As stated in the Claim rejections above, McCaslin discloses receiving a speech signal on each speech path during each sample period and determining far end (column 22, lines 9-10) and near end (column 22, lines 36-38) signal power using peak signal. The speech signals are designated Rin(k) and Sin(k) where k is an index designating a particular sample. As such, every sample on each line is received. Because both signals are sampled at the same rate, there is one far end sample for every near end sample and one near end sample for every far end sample. Since a microprocessor performs operations serially, it will necessarily regularly and alternately receive the two signals.

55. For the reasons stated above, the rejections made in the Office action mailed on 17 February 2004 are maintained.

Conclusion

56. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel Swerdlow whose telephone number is 703-305-4088. The examiner can normally be reached on Monday through Friday between 8:00 AM and 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Forrester Isen can be reached on 703-305-4386. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ds

MINSUN OH HARVEY
PRIMARY EXAMINER